APPLICATION

FOR

UNITED STATES PATENT

Title: Transient Protection Circuit for Darlington Amplifiers

Inventor:

BACKGROUND

1. Field of the Invention

This invention relates to RF and microwave amplifiers in general and more

5   particularly to Darlington gain block amplifiers that have improved biasing to prevent

potentially damaging conditions from occurring. The invention also prevents a voltage

pulse on the output of the amplifier that is formed during the start-up process, which

can damage the circuitry connected to the output of the gain block amplifier.

2. Description of Related Art

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Darlington gain block amplifiers are widely used in RF and microwave systems.

Darlington amplifiers have a frequency range that starts at DC. The biasing conditions

needed by the transistors require de-coupling capacitors at the input and output. The

de-coupling capacitors determine the low end of the amplifier frequency range.

15 Normally, Darlington gain block amplifiers receive a DC bias voltage from an ideal

current source. In practice, the current source is replaced by a voltage source with a

series resistor, which converts it to a reasonably good current source. The resistor

value typically ranges up to a few hundred ohms. Therefore, the DC voltage from the

voltage source can be up to 10 to 15 volts. An optional choke can be connected in

20 series with the resistor to increase the total impedance at the high end of the amplifier

frequency range to minimize gain and power loss.

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Referring to figure 1, a typical Darlington gain block amplifier 12 and biasing

configuration is shown. A pair of NPN transistors Q1 and Q2, are connected in a

Darlington configuration. Transistor Q1 has a base QB1, an emitter QE1 and a collector

QC1. Transistor Q2 has a base QB2, an emitter QE2 and a collector QC2. The emitter

5   QE1 is connected to base QB2. The collectors QC1 and QC2 are connected together.

A biasing network 14 is connected to the amplifier. Biasing network 14 supplies the

proper biasing voltages to transistors Q1 and Q2. Resistor R1 is connected between

base QB1 and collector QC1. Resistor R2 is connected between base QB1 and ground.

Resistor R3 is connected between emitter QE1 and ground. Resistor R4 is connected

10   between emitter QE2 and ground. A 50 ohm resistor R5 and input de-coupling capacitor

C1 are serially connected between base QB1 and ground. 50 ohm resistor R6 and

output de-coupling capacitor C2 are serially connected between the collectors QC1,

QC2 and ground. A controlled current source P1 is connected to the collector QC1,

QC2 junction. The input to the amplifier is on the base QB1. The output from the

15   amplifier is taken from the collector QC2.

If a low frequency response is desired, the de-coupling capacitors C1 and C2

can have a significant value. For example, for a frequency of 100 KHz, the de-coupling

capacitors would have a value around 0.2 uF or more. Where the input and output

impedances are equal to a value of 50 ohms, the input and output de-coupling

20   capacitors normally have the same value.

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Unfortunately, an initial start-up process can result in a dangerous 'voltage bump' or overshoot voltage occurring on the transistors of the Darlington amplifier. In addition to the danger of damaging the Darlington amplifier, the voltage bump can overload and possibly damage the circuitry connected to the output of the Darlington amplifier. The

5   transient process when the current source has a sharp ramp (small rise time) will be detailed next. The worst case is when the current source P1 goes from zero to the nominal current value instantaneously. This would occur if the current source was manually connected such as by plugging in a connector or by turning on a mechanical switch. Initially, the de-coupling capacitors C1 and C2 are not charged and transistors

10   Q1 and Q2 are not conducting.

The initial response of the circuit of figure 1 can be analyzed by using an example of a simplified circuit. Turning to figure 2, a simplified circuit 20 of figure 1 is shown. All the component values in figure 2 are typical values for a Darlington amplifier. Figure 2 has two current probes I1 and I2, current source P1, 510 ohm resistor R1, 580 ohm

15   resistor R2, 50 ohm resistor R5, 50 ohm resistor R6 and 0.2 uF capacitors C1 and C2. Current source P1 has a rise time of 100 nanoseconds. The circuit of figure 2 was analyzed using Agilent ADS 2001 circuit simulator software. When the current source is turned on, capacitors C1 and C2 will begin to charge. However, capacitors C1 and C2 will charge at a differing rate due to the difference in time constants because series

20   resistors R1 + R5 and R6 are different. The total current will be split into two unequal

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parts, initially in a proportion to approximately (R1+R5) / R6.

Figures 3 and 4 show the voltage versus time for the simplified circuit 20 of figure

2 at nodes 'DC out' and 'base', respectively. Figure 5 shows current versus time for

circuit 20 at probes I1 and I2. As seen in figure 5, the current I1 charging C1 is about 10

5   times less than the current charging C2. During charging, the current source split ratio

will change because a larger portion of the current will sink through R1 and R2 directly

to ground. After more than 1 millisecond, C2 will be charged and its charge current I2

will drop to almost zero in figure 5. At this point, input capacitor C1 will also be charged

and all of the 17 milliamps of current will sink through resistors R1 and R2. The total

10   voltage drop across resistors R1 and R2 is 18.5 volts as seen in figure 3 and this is

equivalent to the maximum voltage on node 'DC out'. The voltage drop across resistor

R2 is 9.9 volts as seen in figure 4. This voltage is equivalent to the maximum voltage on

the node 'base' of transistor Q1 of circuit 20.

When transistors Q1 and Q2 are added to the simulated circuit, they will start to

15   conduct when the voltage across R2 reaches 2.6 to 2.8 volts. This is twice the base to

emitter voltage drop (Vbe) for an indium phosphide heterojunction bi-polar transistor (InP

HBT). Transistor Q1 starts to conduct when the node base voltage reaches

approximately 1.3 to 1.4 volts. At this point, the current sinking through transistor Q1

will not be high. Transistor Q2 starts to conduct when the node base voltage reaches

20   approximately 2.6 to 2.8 volts and sinks most of the current. At the time that transistor

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Q2 starts to conduct, the device voltage will already be 7 volts. Therefore, when

transistor Q2 first starts to conduct it will be subjected to the 7 volts peak voltage. Note

that the total peak current through the amplifier of figure 8 exceeds the nominal current

source value of 17 ma because the discharging current of output capacitor C2. If the

5 transistors survive the overvoltage and discharge current conditions, they will shunt the

current until the device voltage drops to a steady value of 5 volts. This is shown in

figures 6-9. Figure 6 shows the total device voltage at node 'DC out' versus time.

Figure 7 shows the amplifier input voltage or the base voltage of input transistor

Q1 versus time.

10 Figure 8 shows the total device current versus time, which includes the current

from the current source and the discharge current from output capacitor C2. This can

be more than the total current source current.

Figure 9 shows the emitter currents through transistors Q1 and Q2 versus time.

The most dangerous moment for the transistors is when the total device voltage

15 reaches a maximum value (marker M5 in figure 6) and transistor Q2 starts to conduct

(marker M4 in figure 9). The total device voltage is about 6.85 volts at this moment.

Figures 10-13 show actual oscilloscope measurements on a circuit of figure 1 that

was built. A Keithley 236 power supply was used for the current source. An Infiniium

HP 54035A oscilloscope from Agilent was used to measure the voltage versus time for

20 various current source values. Figure 10 shows the output voltage versus time for a

current source of 11 milli-amps. Figure 11 shows the output voltage versus time for a current source of 12 milli-amps. Figure 12 shows the output voltage versus time for a current source of 13 milli-amps. Figure 13 shows the output voltage versus time for a current source of 14 milli-amps.

5   Figures 10-13 show how quickly the amplifier peak voltage rises with an increase in the current source value. As seen in figure 13, permanent damage to the output transistors of the amplifier occurred with a current source value of 14 milli-amps. The amplifier device voltage does not come to a steady 5 volt value. Sequential gain measurements confirm that the amplifier is permanently damaged.

10   This problem only exists for a current source with small rise times. For a slow current source, the charging rate of the input capacitor C1 and output capacitor C2 are about the same and determined mostly by the long rise time of the current source. Therefore the output voltage will not have the peaking shape and the voltage overshoot or voltage bump problem does not occur. With a slow current source, the amplifier can

15   typically handle up to 51 milli-amps of current. Therefore, the overshoot problem is a pure transient issue at start up. It is not a steady state power dissipation limit problem.

While various Darlington transistor biasing schemes have previously been used, they have suffered from not being able to adequately protect against destructive transient voltage overshoot conditions and from interfering with normal amplifier

20   operation. A current unmet need exists for an improved Darlington amplifier biasing

circuit that is low in cost, protects against destructive transient voltage overshoot conditions and does not interfere with normal amplifier operation.

SUMMARY

5   It is a feature of the invention to provide a Darlington amplifier circuit that prevents destructive transient voltage overshoot conditions from occurring.

Another feature of the invention is to provide an amplifier circuit that includes a first transistor having a first base, a first collector and a first emitter. A second transistor has a second base, a second collector and a second emitter. The emitter of the first

10   transistor is connected to the base of the second transistor. The collector of the first transistor is connected to the collector of the second transistor. A first resistor is connected between the collector of the first transistor and the base of the first transistor. A second resistor is connected between the base of the first transistor and ground. A first capacitor is connected to the base of the first transistor. A second capacitor is

15   connected to the collectors of the first and second transistors. The second capacitor has a capacitance value at least 5 times larger than the first capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a prior art Darlington gain block amplifier.

20   Figure 2 is a schematic of a simplified circuit of figure 1.

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Figure 3 is a graph of voltage at node 'dc out' versus time for the simplified circuit 20 of figure 2.

Figure 4 is a graph of voltage at node 'base' versus time for the simplified circuit 20 of figure 2.

5 Figure 5 is a graph of current versus time for the simplified circuit 20 of figure 2 showing charging of capacitors C1 and C2.

Figure 6 is a graph of the total amplifier device voltage versus time for circuit 12 of figure 1.

Figure 7 is a graph of the amplifier input voltage or the base voltage of transistor 10 Q1 versus time for circuit 12 of figure 1.

Figure 8 is a graph of the total device current versus time for circuit 12 of figure 1.

Figure 9 is a graph of the emitter currents IQ1 and IQ2 through transistors Q1 and Q2 versus time for circuit 12 of figure 1.

Figure 10 is a graph of the oscilloscope measurement of the amplifier output 15 voltage versus time for a current source of 11 milli-amps for circuit 12 of figure 1.

Figure 11 is a graph of the oscilloscope measurement of the amplifier output voltage versus time for a current source of 12 milli-amps for the circuit 12 of figure 1.

Figure 12 is a graph of the oscilloscope measurement of the amplifier output voltage versus time for a current source of 13 milli-amps for the circuit 12 of figure 1.

20 Figure 13 is a graph of the oscilloscope measurement of the amplifier output

voltage versus time for a current source of 14 milli-amps for the circuit 12 of figure 1.

Figure 14 is a graph of the total amplifier device voltage versus time for circuit 12 of figure 1 and the value of C2 is 5 times larger than C1.

Figure 15 is a graph of the amplifier input voltage or the base voltage of transistor

5   Q1 versus time for circuit 12 of figure 1 and the value of C2 is 5 times larger than C1.

Figure 16 is a graph of the total device current versus time for circuit 12 of figure 1 and the value of C2 is 5 times larger than C1.

Figure 17 is a graph of the emitter currents IQ1 and IQ2 through transistors Q1 and Q2 versus time for circuit 12 of figure 1 and the value of C2 is 5 times larger than

10   C1.

Figure 18 is a graph of the total amplifier device voltage versus time for circuit 12 of figure 1 and the value of C2 is 10 times larger than C1.

Figure 19 is a graph of the amplifier input voltage or the base voltage of transistor Q1 versus time for circuit 12 of figure 1 and the value of C2 is 10 times larger than C1.

15   Figure 20 is a graph of the total device current versus time for circuit 12 of figure 1 and the value of C2 is 10 times larger than C1.

Figure 21 is a graph of the emitter currents IQ1 and IQ2 through transistors Q1 and Q2 versus time for circuit 12 of figure 1 and the value of C2 is 10 times larger than C1.

20   Figure 22 is a graph of the total amplifier device voltage versus time for circuit 12

of figure 1 and the value of C2 is 484 times larger than C1.

Figure 23 is a graph of the amplifier input voltage or the base voltage of transistor Q1 versus time for circuit 12 of figure 1 and the value of C2 is 484 times larger than C1.

Figure 24 is a graph of the total device current versus time for circuit 12 of figure 1 and the value of C2 is 484 times larger than C1.

Figure 25 is a graph of the emitter currents IQ1 and IQ2 through transistors Q1 and Q2 versus time for circuit 12 of figure 1 and the value of C2 is 484 times larger than C1.

Figure 26 is a graph of the actual oscilloscope measurement of the amplifier output voltage versus time for circuit 12 of figure 1 that was built with C1 = 0.013 uF and C2 = 6.3 uF (C2 is 484 times larger than C1).

Figure 27 is a schematic diagram of an alternative embodiment of the present invention.

Figure 28 is a graph of the total amplifier device voltage versus time for circuit 200 of figure 27.

Figure 29 is a graph of the amplifier input voltage or the base voltage of transistor Q1 versus time for circuit 200 of figure 27.

Figure 30 is a graph of the total device current versus time for circuit 200 of figure 27.

Figure 31 is a graph of the emitter currents IQ1 and IQ2 through transistors Q1

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and Q2 versus time for circuit 200 of figure 27.

Figure 32 is a graph of the currents IR1 through resistor R1 and currents ID1, ID2

through diodes D1 and D2 versus time for circuit 200 of figure 27.

Figure 33 is a schematic diagram of another embodiment of the present

5   invention.

Figure 34 is a graph of the total amplifier device voltage versus time for circuit

300 of figure 33.

Figure 35 is a graph of the amplifier input voltage or the base voltage of transistor

Q1 versus time for circuit 300 of figure 33.

10   Figure 36 is a graph of the total device current versus time for circuit 300 of figure

33.

Figure 37 is a graph of the emitter currents IQ1 and IQ2 through transistors Q1

and Q2 versus time for circuit 300 of figure 33.

Figure 38 is a graph of the current IR1 through resistor R1 and current IQ3

15   through transistor Q3 versus time for circuit 300 of figure 33.

Figure 39 is a schematic diagram of another embodiment of the present

invention.

It is noted that the drawings of the invention are not to scale. In the drawings,

like numbering represents like elements between the drawings.

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DETAILED DESCRIPTION

One possible way to prevent the voltage overshoot problem on transistors Q1 and Q2 is to use a slow power supply at start-up. This solution to use a special power supply is not practical for most applications. In many cases, slow start up is not

5   acceptable from the overall system requirements and restrictions. It is also expensive to design this type of power supply.

The voltage overshoot on transistors Q1 and Q2 at start up can be controlled by varying the capacitance ratio of capacitor C2 to C1. The ratio C2/C1 should be equal or greater than (R1+R5)/R6. This will equalize the time constant of C1*(R1+R5) and

10   C2*R6 and therefore equalize the charging rate of capacitors C1 and C2. For the given example, If the value of C2 is made 5 to 10 times larger than the value of C1, the voltage overshoot on transistors Q1 and Q2 can be prevented.

Referring to figures 14-17, a simulation is shown for circuit 12 of figure 1 with the value of capacitor C2 five times larger than C1. Figure 14 is a graph of the total

15   amplifier device voltage versus time. The 'voltage bump' or overshoot in figure 14 is much less than that in figure 6 where the value of capacitors C1 and C2 are equal. Figure 15 is a graph of the amplifier input voltage or the base voltage of transistor Q1 versus time for circuit 12 of figure 1. Figure 16 is a graph of the total device current versus time for circuit 12 of figure 1. There is no 'current bump' or current overshoot in

20   figure 16 compared with the significant 'current bump' shown in figure 8 where the

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values of capacitors C1 and C2 are equal. The graph of figure 16 shows that capacitor C2 does not accumulate an extra charge, which can discharge through transistor Q2 as it turns on causing damage.

Figure 17 shows a graph of the emitter currents IQ1 and IQ2 through transistors Q1 and Q2 versus time for circuit 12 of figure 1. As can be seen in figure 17, the current IQ2 through transistor Q2 does not have the 'current bump' because capacitor C2 does not accumulate extra charge.

Referring to figures 18-21, a simulation is shown for circuit 12 of figure 1 with the value of capacitor C2 ten times larger than C1. The ratio of C2/C1 is approximately equal to (R1+R5)/R6. Figure 18 is a graph of the total amplifier device voltage versus time. The 'voltage bump' or overshoot voltage effect is further reduced. Figure 19 is a graph of the amplifier input voltage or the base voltage of transistor Q1 versus time for circuit 12 of figure 1. Figure 20 is a graph of the total device current versus time for circuit 12 of figure 1. The 'current bump' has been eliminated. Figure 21 is a graph of the emitter currents IQ1 and IQ2 through transistors Q1 and Q2 versus time for circuit 12 of figure 1. As can be seen in the graphs, the 'current bump' through transistor Q2 and therefore through the amplifier is eliminated. The 'voltage bump' or overshoot is also eliminated.

Referring to figures 22-25, a simulation is shown for circuit 12 of figure 1 with the value of capacitor C2 484 times larger than C1. In this case, the ratio of capacitor C2 to

14

C1 is further increased and the ratio is much more than (R1+ R5)/R6. In this example

C1 = 0.013 uF and C2 = 6.3 uF. Figure 22 is a graph of the total amplifier device

voltage versus time for circuit 12 of figure 1. There is no 'voltage bump' or overshoot

present. Figure 23 is a graph of the amplifier input voltage or the base voltage of

5   transistor Q1 versus time for circuit 12 of figure 1. Figure 24 is a graph of the total

device current versus time for circuit 12 of figure 1. There is no 'current bump' or

overshoot present. Figure 25 is a graph of the emitter currents IQ1 and IQ2 through

transistors Q1 and Q2 versus time for circuit 12 of figure 1. As can be seen in figures

22-25, increasing the ratio of capacitor C2 to C1, beyond the ratio of (R1+R5)/R6 slightly

10   reduces the already insignificant voltage overshoot that was shown in figures 18-21.

Figure 26 shows an actual oscilloscope measurement for the circuit 12 of figure 1

that was built with C1 = 0.013 uF and C2 = 6.3 uF. Figure 26 shows that the overshoot

problem has been eliminated.

Varying the ratio of the input de-coupling capacitor to the output decoupling

15   capacitor can be done for various Darlington amplifier configurations other than those

shown in figure 1. This technique can also be applied to non Darlington amplifier

configurations including but not limited to pulse amplifiers and video amplifiers.

Turning now to figure 27, another embodiment of the present invention is shown.

Darlington amplifier circuit 200 has been modified from that shown in figure 1. In circuit

20   200, a pair, for example, of serially connected diodes D1 and D2 have been connected

across resistor R1. There can be a single diode, a pair or more diodes connected in series. The number of diodes determines the level of protection of the amplifier. Diodes D1 and D2 are shown as transistors connected as diodes. The emitter of D1 is connected to the base QB1 and resistor R1 junction. The collector of D2 is connected

5   to the collector QC1, resistor R1 junction. The total voltage drop across the diodes D1 and D2 is slightly higher than the voltage drop across resistor R1 in a steady state. At the beginning of the voltage overshoot, the voltage drop across resistor R1 increases above the steady state voltage drop on it and will exceed the opening voltage of the diode pair D1 and D2. At this point, diodes D1 and D2 start to conduct a current and

10   provide some additional current causing capacitor C1 to charge faster. This prevents the overshoot voltage. In the steady state, diodes D1 and D2 do not conduct and are not interfering with the normal RF operation of the amplifier.

Figures 28-32 show simulated results for circuit 200 in figure 27. Figure 28 is a graph of the total amplifier device voltage versus time for circuit 200 of figure 27. The

15   'voltage bump' is significantly less than in figure 6. Figure 29 shows a graph of the amplifier input voltage or the base voltage of transistor Q1 versus time for circuit 200 of figure 27. Figure 30 is a graph of the total device current versus time for circuit 200 of figure 27. The current bump or overshoot current is significantly less than in figure 8. Figure 31 is a graph of the emitter currents IQ1 and IQ2 through transistors Q1 and Q2

20   versus time for circuit 200 of figure 27. The 'current bump' through transistor Q2 is

significantly less than that shown in figure 9. Figure 32 is a graph of the current IR1

through resistor R1 and ID1, ID2 through diodes D1 and D2 versus time for circuit 200 of

figure 27. The peak current ID1, ID2 is almost same value as the peak current IR1

through the resistor R1. Therefore, the total peak current charging capacitor C1 is

5   almost double the value shown in the circuit of figure 1. As can be seen in figures 28-

31, the overshoot problem is significantly reduced by circuit 200 as compared to circuit

12.

Turning now to figure 33, another embodiment of the present invention is shown.

Darlington amplifier circuit 300 of figure 33 has been modified from that shown in figure

10   1. In circuit 300, a third transistor Q3 has been connected across resistor R1.

Transistor Q3 has a base QB3, an emitter QE3 and a collector QC3. The emitter of

transistor Q3 is connected to the junction of base QB1 and resistor R1. The collector of

transistor Q3 is connected to the junction of collector QC1 and resistor R1. The base of

transistor Q3 is connected to a voltage divider consisting of resistors R7 and R8.

15   Resistor R7 is connected to node the junction of collector QC1, QC3 and resistor R1.

Resistor R8 is connected to ground. The ratio of resistors R7 and R8 is chosen based

on the maximum required RF peak voltage on the output of the amplifier. The RF peak

voltage at the 1 dB compression point determines the resistor R7, R8 division ratio.

The resistor R7, R8 division ratio should be set such that the 1 dB compression

20   point degrades by only 0.1 to 0.2 dB at low frequencies with reference to the 1 dB

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compression point of the same amplifier but without the protective circuit.

In the steady state, transistor Q3 is not conducting because the voltage on the base of transistor Q3 set by the voltage divider of R7 and R8 is less than the opening voltage Vbe for transistor Q3. Therefore, transistor Q3 does not interfere with the

5   normal RF operation of the amplifier.

During the start up process, the voltage on the base of transistor Q3 increases, turning on transistor Q3, which causes capacitor C1 to charge faster. This prevents the overshoot voltage problem. The circuit 300 of figure 33 has the added convenience and ability to finely adjust the voltage protective level by varying the values of resistors R7

10   and R8. As a side effect, the 1dB compression point of the amplifier may be slightly degraded by about 0.2 dB less.

Figures 34-38 show simulated results for circuit 300. Figure 34 shows a graph of total amplifier device voltage versus time for circuit 300 of figure 33. The 'voltage bump' is further reduced as compared to that shown in figure 28. Figure 35 is a graph of the

15   amplifier input voltage or the base voltage of transistor Q1 versus time for circuit 300 of figure 33. Figure 36 is a graph of the total device current versus time for circuit 300. The 'current bump' is further reduced from that shown in figure 30.

Figure 37 shows a graph of the emitter currents IQ1 and IQ2 through transistors Q1 and Q2 versus time for circuit 300 of figure 33. The 'current bump' through

20   transistor Q2 as well as the 'total bump' of the total amplifier current is significantly less

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than in figure 31. Figure 38 is a graph of the current IR1 through resistor R1 and current

IQ3 through transistor Q3 versus time for circuit 300. The peak current IQ3 is almost

the same value as the peak current IR1 through resistor R1. Therefore, the total peak

current charging capacitor C1 is almost double that shown in circuit 12 of figure 1.

5   As can be seen in figures 34-37, the overshoot problem is significantly reduced

by circuit 300.

        Referring to figure 39, another embodiment of the present invention is shown.

Darlington amplifier circuit 400 has been modified from that shown in figure 1. In circuit

400, transistor Q4 has been connected in parallel across transistor Q1. Transistor Q4

10   has a base QB4, an emitter QE4 and a collector QC4. The emitter QE4 of transistor Q4

is connected to the emitter QE1 of Q1. The collector QC4 of transistor Q4 is connected

to the collector QC1 of Q1. The base QB4 of transistor Q4 is connected to a voltage

divider consisting of resistors R7 and R8. Resistor R7 is connected to the collectors of

Q1 and Q4. Resistor R8 is connected to ground.

15   The ratio of resistors R7 and R8 is chosen based on the maximum required RF

peak voltage on the output of the amplifier. The RF peak voltage at the 1 dB

compression point determines the resistor R7, R8 division ratio.

        The resistor R7, R8 division ratio should be set such that the 1 dB compression

point degrades by only 0.1 to 0.2 dB at low frequencies with reference to the 1 dB

20   compression point of the same amplifier but without the protective circuit.

During steady state operation, transistor Q4 does not interfere with the normal RF operation of the amplifier because the base to emitter voltage of transistor Q4, which is set by the resistor divider R7, R8 is below the voltage required to open transistor Q4.

It is noted that circuit 200 would have the least influence on the RF performance of the Darlington amplifier. The circuit changes shown in circuits 200 and 300 can be readily implemented on existing Darlington amplifiers by adding external circuitry. These circuit changes can also be implemented on a semiconductor die during fabrication.

The present invention has several advantages. Changing the ratio of the input to output de-coupling capacitors provides a solution to the problem of voltage overshoot on Darlington amplifiers without extra space needs and the expense of additional components. The three circuit modifications that were shown can also be readily implemented at low cost and uses a minimum amount of additional circuit board space to prevent voltage overshoot on Darlington amplifiers. The invention provides an increase in Darlington amplifier reliability and durability at low cost.

While the invention has been taught with specific reference to these embodiments, someone skilled in the art will recognize that changes can be made in form and detail without departing from the spirit and the scope of the invention. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than

by the description. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.